OIPE
JUN 09 2004
PATENT & TRADEMARK OFFICE
JC130

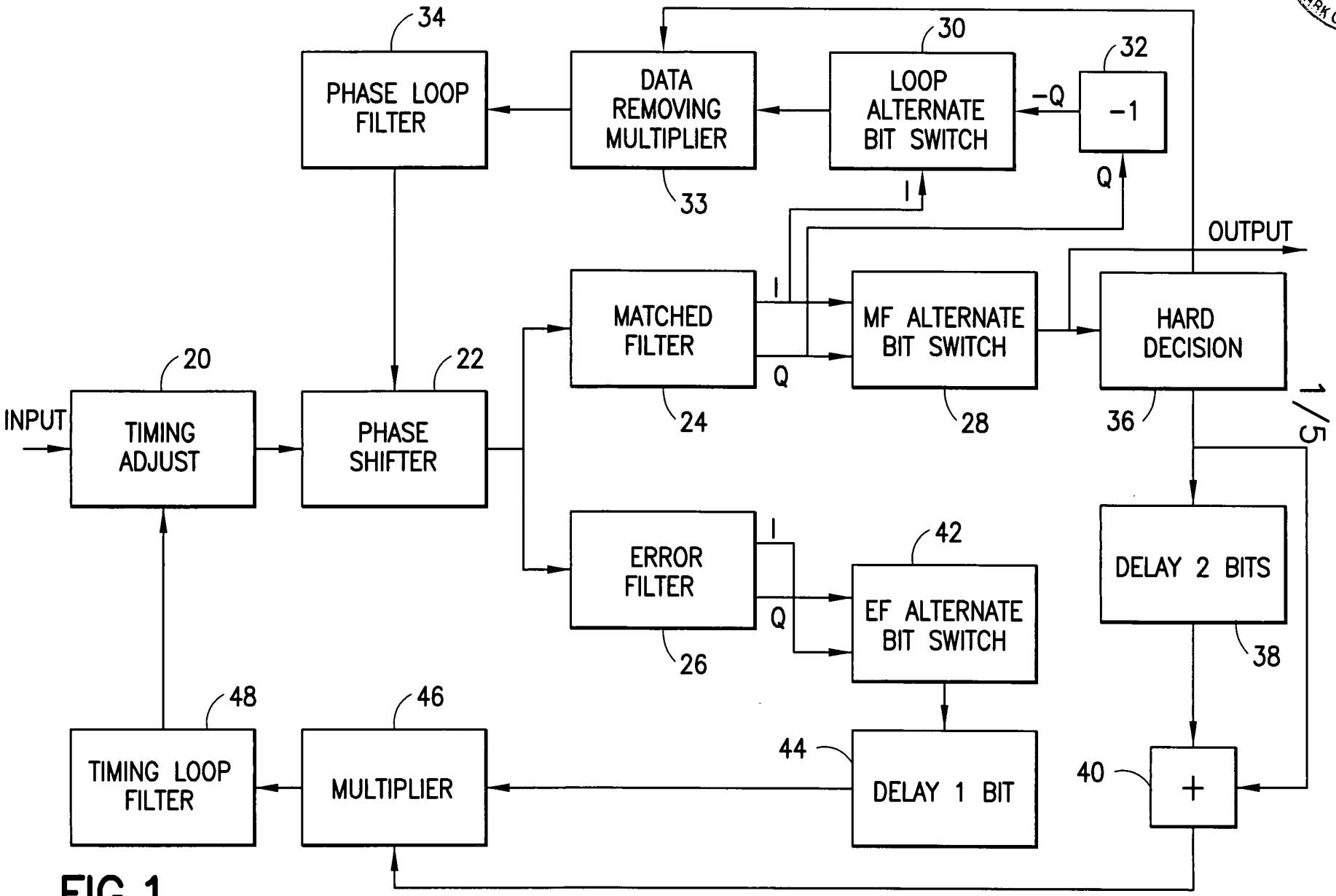

FIG.1
PRIOR ART

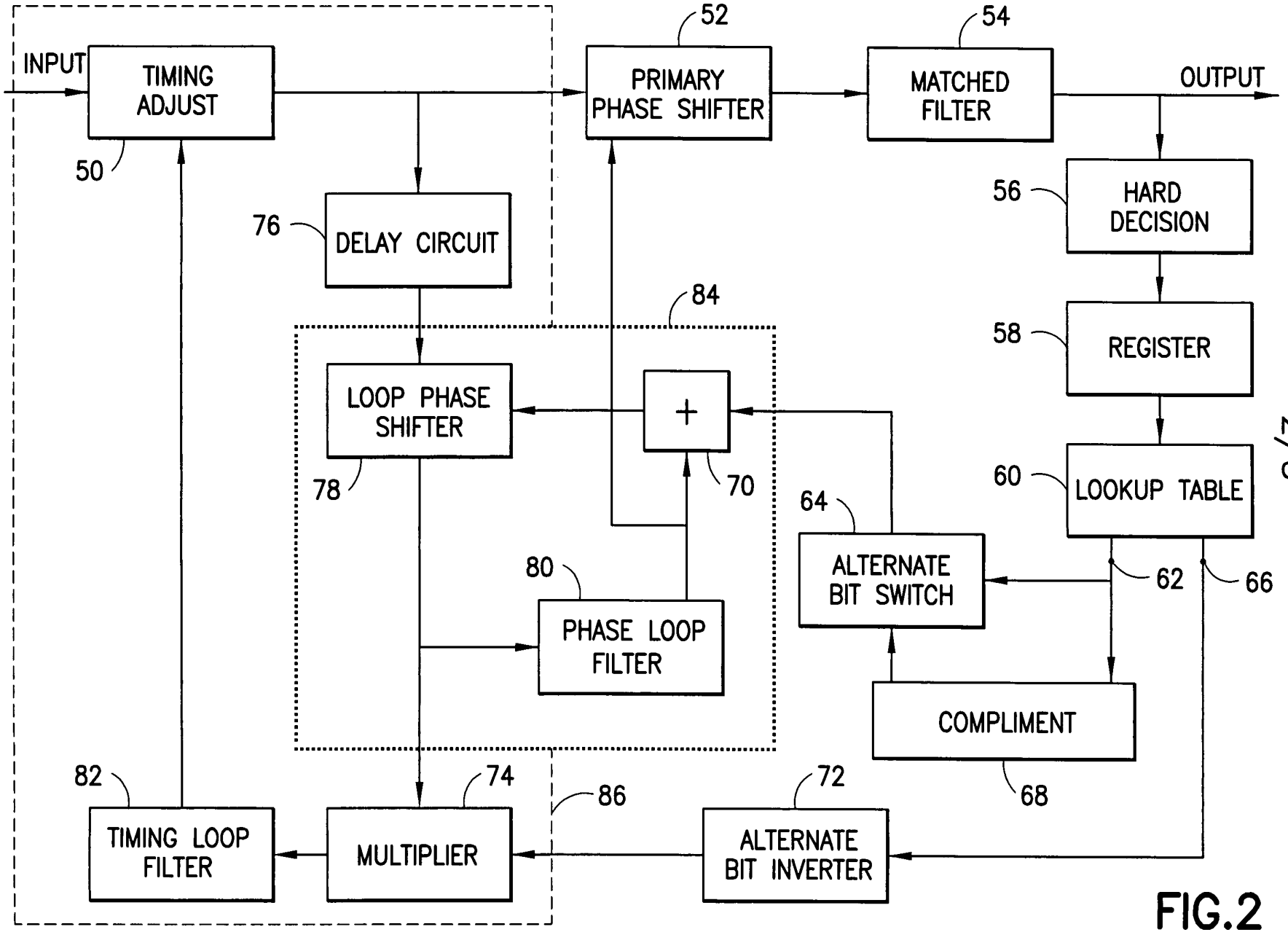
INPUT
TIMING ADJUST
50
PRIMARY PHASE SHIFTER
52
MATCHED FILTER
54
OUTPUT
HARD DECISION
56
REGISTER
58
LOOKUP TABLE
60
62
66
ALTERNATE BIT SWITCH
64
COMPLIMENT
68
ALTERNATE BIT INVERTER
72
DELAY CIRCUIT
76
84
LOOP PHASE SHIFTER
78
+
70
PHASE LOOP FILTER
80
TIMING LOOP FILTER
82
MULTIPLIER
74
86

FIG.2

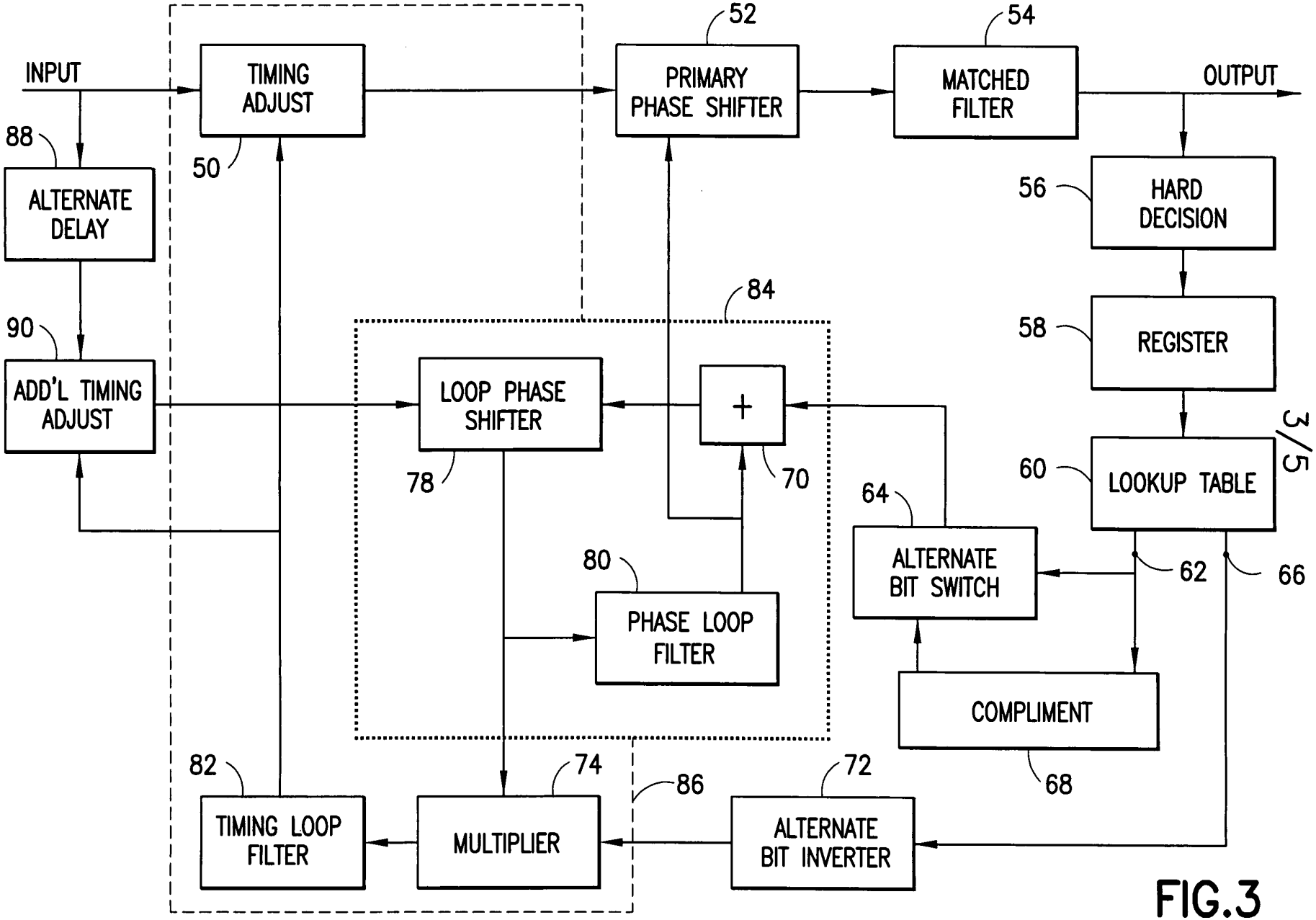
INPUT
TIMING ADJUST
50
52
PRIMARY PHASE SHIFTER
54
MATCHED FILTER
OUTPUT
88
ALTERNATE DELAY
56
HARD DECISION
84
90
ADD'L TIMING ADJUST
LOOP PHASE SHIFTER
+
58
REGISTER
78
70
60
LOOKUP TABLE
3/5
64
ALTERNATE BIT SWITCH
62
66
80
PHASE LOOP FILTER
COMPLIMENT
68
82
TIMING LOOP FILTER
74
MULTIPLIER
86
72
ALTERNATE BIT INVERTER

FIG.3

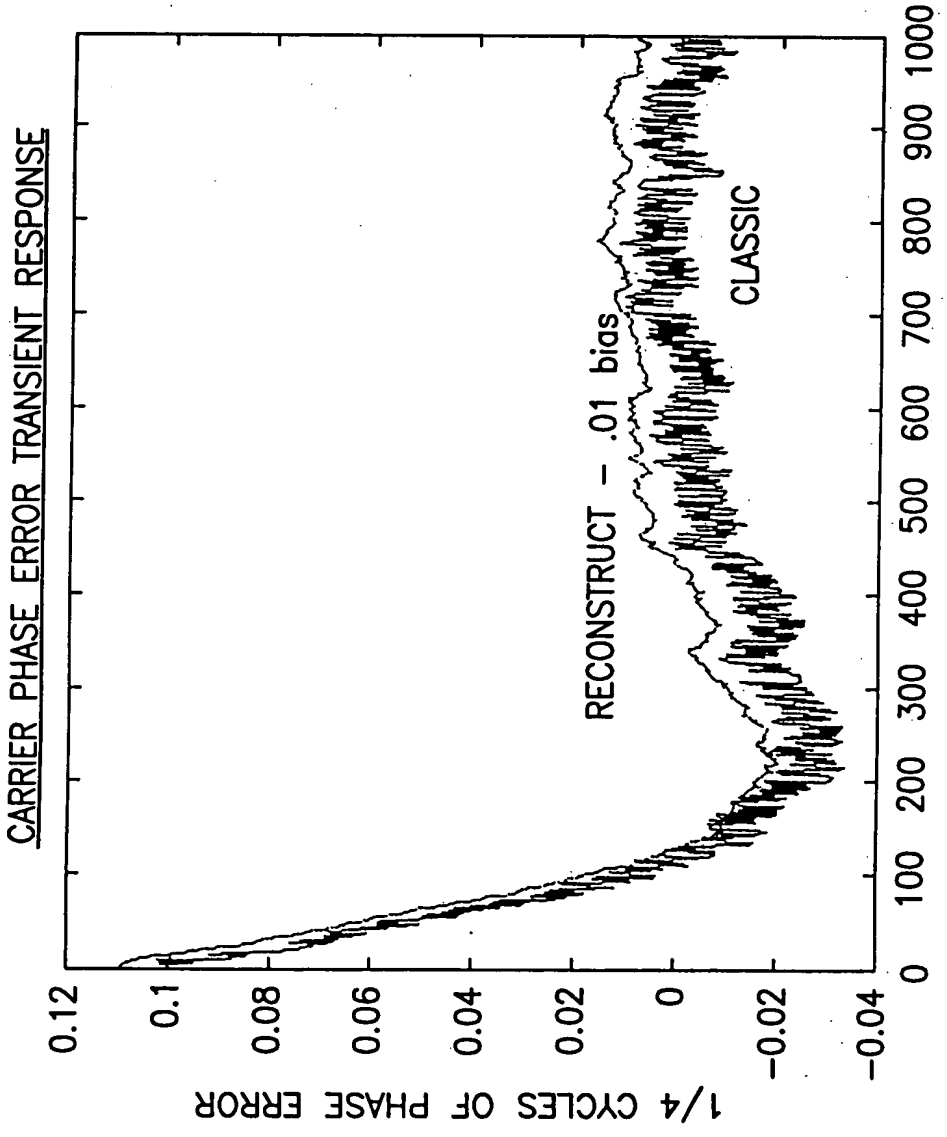
CARRIER PHASE ERROR TRANSIENT RESPONSE
RECONSTRUCT – .01 bias
CLASSIC
1/4 CYCLES OF PHASE ERROR
BIT TIME
0.12
0.1
0.08
0.06
0.04
0.02
0
−0.02
−0.04
0
100
200
300
400
500
600
700
800
900
1000

FIG.4

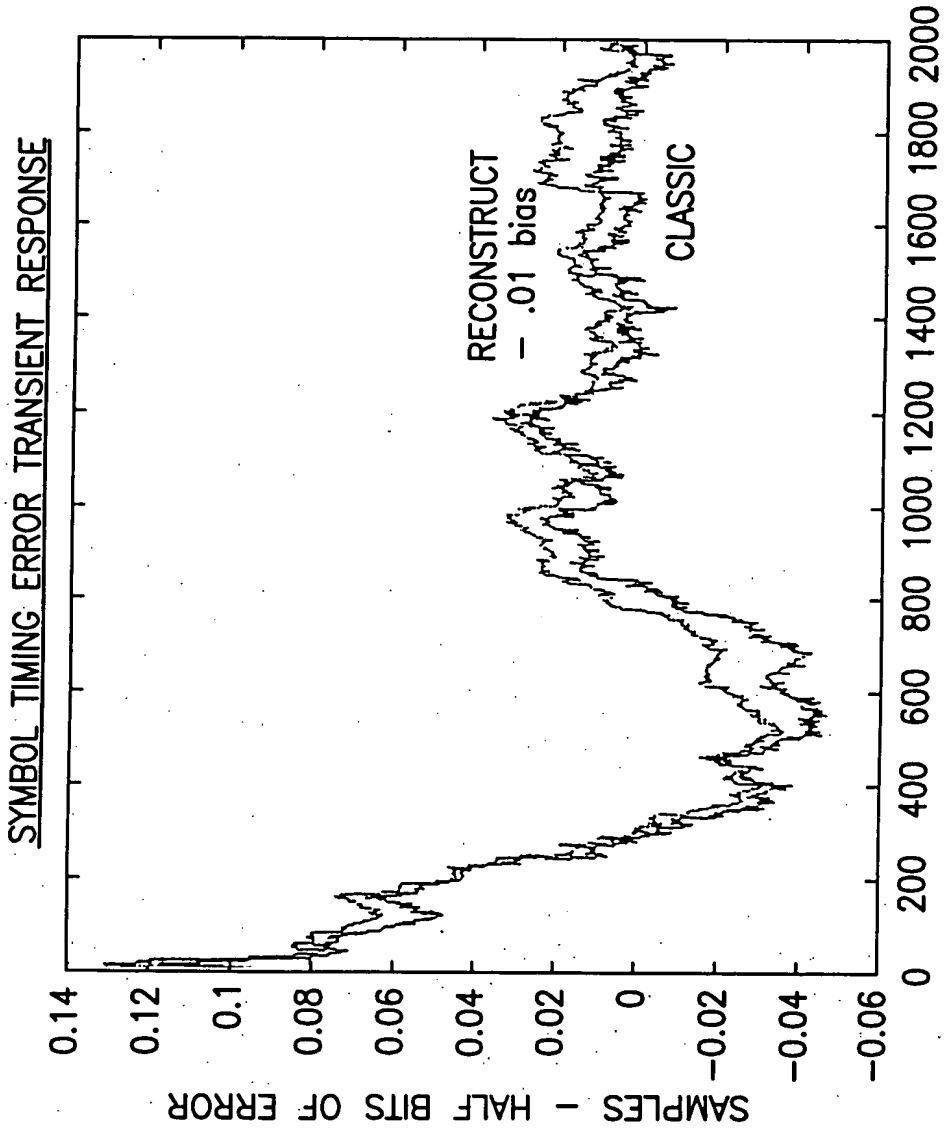
SYMBOL TIMING ERROR TRANSIENT RESPONSE
RECONSTRUCT
– .01 bias
CLASSIC
SAMPLES – HALF BITS OF ERROR
BIT TIME
0.14
0.12
0.1
0.08
0.06
0.04
0.02
0
−0.02
−0.04
−0.06
0
200
400
600
800
1000
1200
1400
1600
1800
2000

FIG.5